Customer No.: 31561
Application No.: 10/604,692
Docket No.: 10156-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A split-gate non-volatile memory cell, comprising:

a substrate;

a charge-trapping layer on the substrate;

a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer; and

a source/drain in the substrate beside the split gate, wherein

the charge-trapping layer around the split region serves as a coding region.

2. (original) The split-gate non-volatile memory cell of claim 1, wherein the split gate consists of at least two pieces separated by a dielectric layer.

3. (original) The split-gate non-volatile memory cell of claim 2, wherein the split gate consists of three pieces.

4. (original) The split-gate non-volatile memory cell of claim 3, wherein the three pieces of the split gate include a pair of conductive spacers and a conductive layer between the pair of conductive spacers.

5. (original) The split-gate non-volatile memory cell of claim 4, wherein the pair of conductive spacers are arranged with two substantially vertical sidewalls thereof adjacent to the source/drain.

6. (original) The split-gate non-volatile memory cell of claim 5, further

comprising an insulator on the source/drain, wherein the pair of conductive spacers are disposed on the sidewalls of the insulator.

7. (original) The split-gate non-volatile memory cell of claim 2, wherein different pieces of the split gate are electrically connected to each other.

8. (original) The split-gate non-volatile memory cell of claim 2, wherein the dielectric layer comprises silicon oxide.

9. (original) The split-gate non-volatile memory cell of claim 1, wherein the split gate comprises polysilicon.

10. (original) The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises a silicon nitride layer disposed between two silicon oxide layers.

11. (original) The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises aluminum oxide (Al_2O_3).

12. (original) The split-gate non-volatile memory cell of claim 1, wherein the substrate comprises a p-substrate, and the source/drain comprises an n-type source/drain.

13.-34. (cancelled).

35. (original) An operating method of a split-gate non-volatile memory cell, wherein

the split-gate non-volatile memory cell comprises:

a substrate;

a charge-trapping layer on the substrate;

a split gate on the charge-trapping layer, including at least one split region

directly over the charge-trapping layer, wherein the charge-trapping layer around the split region serves as a coding region; and

a source/drain in the substrate beside the split gate, and

the operating method comprises:

in a programming operation:

applying 0V to the substrate and the source/drain; and

applying a first negative voltage to the split gate, the first negative voltage being sufficiently high for injecting electrons into the coding region; and

in an erasing operation:

applying 0V to the split gate;

floating the source/drain; and

applying a second negative voltage to the substrate, the second positive voltage being sufficiently high for ejecting electrons from the coding region.

36. (original) The operating method of claim 35, wherein the first negative voltage is about –10V.

37. (original) The operating method of claim 35, wherein the second negative voltage is about –10V.

38.-45. (canceled)